Examples of the endless possibilities in the field of Microscopy

Through Silicon Vias (TSVs) were cleaved near to the center and then polished using Focus Ion Beam (FIB). The combination of those two operations created a good surface to reveal grain structure in tungsten and provides suitable low surface roughness for EBSD and EDS analysis. Images from: Advances in FIB-SEM Analysis of TSV and Solder Bumps - Approaching Higher Precision, Throughput and Comprehensiveness, Hrncir et al., ISTFA 2014

Sapphire wafers cleaved along crystalline directions, No-Scribe approach leads to clean debris-free surfaces and yields cross-sections with mirror-finish facets.
EMS MICROSCOPY ACADEMY
SAMPLE PREPARATION FOR SEMICONDUCTOR DEVICES:
A COMPLETE PICTURE

Successful analysis is based on the accuracy, quality and efficiency of sample preparation!

- Do you need to prepare samples for characterization, process development, failure analysis, or process monitoring?
- Do you want to add sample prep to your skill-set in characterization of semiconductor devices on wafer, die and/or package level?
- Are you working in a lab that requires you to be proficient in sample preparation for semiconductor devices?

If the answer is yes to any of those questions, then this is the class for you!

- In three days, we will present the background theory, current methods, tools and the workflow selection process, as well as provide hands on experience in aspects of wafer downsizing, sample cross-sectioning, device delayering, and extraction.

Details

Tuesday - Thursday
January 15 - 17, 2019
8:30 a.m. - 4:30 p.m.
Hatfield, Pennsylvania, USA

Targeted Participants

Individuals who are, or soon will be, expected to prepare specimens and/or perform characterization of semiconductor devices with Optical Microscopy, SEM, or FIB; as well as individuals who may be experienced in other types of material analysis work, but are new to the field of semiconductor device sample preparation for reliability, research, and failure analysis. This workshop is appropriate for managers/supervisors, engineers and technicians working with samples of Thin Films on crystalline or amorphous substrates, such as those utilized in Semiconductor Industry, LED, Flat Panel Displays (LCD,) Photo Voltaic Devices, and Electronics, or analysts engaged in IP-Legal Discovery support services, as well as for University researchers that need to prepare routine specimens from multilayers and thin films.

The EMS Microscopy Academy

Located in Hatfield, Pennsylvania, the Academy provides electron microscopy classes, workshops and training sessions for all fields of microscopy, including materials science and biological science.
Scope of Class

This course covers sample preparation required for isolation of devices, circuit components, and defects on semiconductor wafers and loose die extracted from packages. These preparation steps are essential for further processing or analysis in SEM, FIB, TEM or Optical Microscopy.

The sample preparation process starts with defining the purpose of analysis, the desired outcome of sample preparation, and planning of the workflow: selecting hand tools and equipment, choosing appropriate consumables, and performing the preparation in a way that final specimen is still representative of the features in the actual device.

Often, multiple techniques such as: Optical Microscopy, SEM (or FIB/SEM) imaging are used in course of analysis. Details of the structure or defect can be elucidated with Energy Dispersive X-Ray Spectroscopy or Auger Spectroscopy. Accurate characterization and analysis depend on the sample preparation workflow selection and the execution to successfully retain original structure while sizing it, cross-section it and/or removing layers to uncover the feature of interest.

Every workflow starts with identification (ID) and marking of the area of interest (AOI,) the target to be characterized. This ID process can be done by unaided eye, under optical microscope, through electrical testing or SEM. Marking of AOI can be done by ink, scriber, laser or FIB, the goal is to clearly identify the target for further processing steps, and to do so in a way that is compatible with further preparation process.

The first part of the course will introduce students to the handling of semiconductor or thin film substrates, introduce common themes in device design layout and test structure locations, discuss features of microelectronic and IC devices, and provide strategies for sample preparation procedures for analyzing semiconductor devices on a micro-scale.

The second part of this Course will be focused on extraction of die from packages and further preparation steps. Preparation of Semiconductor packaging specimens are drastically different from the usual bulk materials sample handling. This course will give participants an overview of the types of semiconductor packages, package construction, die access techniques, sample preparation requirements, basic fail site location methods, etchant recipes, and cross-section parameters. In addition, it will provide tips and tricks needed to perform physical failure analysis of packaged semiconductor devices. The challenges associated with such specimens are unique and require combination of physical de-structuring of the package, as well as dealing with an integrated circuit on substrates of reduced thickness that are extremely fragile. The course will introduce strategies and provide examples of physical, thermally assisted, and chemical device extraction of die for analysis.
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After instructional sessions, the remainder of time will be spent in the lab, observing and then practicing hands-on sample preparation under guidance of the instructors. In that portion of each class, you will learn the background necessary to design the best prep workflow based on the desired outcome, prepare specimens from wafers and amorphous substrates, identify common features, and avoid common pitfalls, while handling these devices.

Format

Lecture, demonstration and guided hands-on practice, as well as round table discussion. Participants are encouraged to bring their own samples, if possible. For example, these skills can be practiced on a Familiar semiconductor device or suitable electronic device, eg:

- Used, or older USB Flash Memory stick <4GB, or a Compact Flash Card, or a RAM stick
- Non-proprietary wafers with printed devices and scribe line test structures (some obsolete devices are available on E-Bay).

Main Curriculum

Day 1: Packaged Devices

Lecture 1: Device packaging overview - types and construction.
Lecture 2: Gaining access to the die - extraction strategies.
Lecture 3: Common tools, laboratory safety, preparation, and accessing the fail site.

Day 2: Devices on Wafer and Die Level

Lecture 1: Seeking targets - Process Technology Background

- Manufacturing of semiconductor devices
- Wafers and substrates - crystallography and process technology: from diffusion to bump
- Device layouts, wafer test structures, and common die components
- Packaged Die and Internal Components/Interconnects
- Overview of Laboratory Equipment and Tools: from Thumb to FIB
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Lecture 2: Laboratory strategies and de-process overview

- De-processing strategies for common tasks
- Plan View Layout Extraction: cells and modules Layer and Component Metrology
- Device Physics and Composition of Layers
- Prep for Device Edit and Probing (FIB processing) Cross-sections and Physical Deprocessing
- Wafer Cleaving
- Mechanical Gridding and Polishing Intro to FIB cleanup and chemical etch

Lecture 3: Common Tools in Sample Prep

- Chemical Deprocessing
- Heat, Wet Chemicals, and Safety Reactive Ion Etch
- Plasma Cleaning
- Specimen preparation for microscopy and FIB: Sample mounting and processing Cleaning and etching
- Coatings: Protective layers and highlights: SOG vs. CVD vs. PVD dep Review of common lab tools, materials, and safety topics

Day 3: Hands-On Self Practice Laboratory (under guidance of instructors)

- Students will work under guidance of instructor to practice techniques and prepare cross-section of a device they brought to the course. Extracted die or wafer piece is recommended.

Day 1 and Day 2: Demonstration Laboratory Sessions

Lab 1 (45 min): Demonstration of die retrieval.
Lab 2 (3 hrs): Guided Practice: Students will attempt to extract die from common packaging or a specimen they bring to the course.
- Demonstration of tools for wafer level work
- Manual wafer level prep with hand scribe and LatticeAx™
- Automated tools for laboratory - die cutting, wafer cleaving, device polishing
- Marking and Coating
- Polishing tools and plane view sections; SEM metrology demo
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Instruments Available

| General Laboratory tools for sample prep, mounting, and polishing | Handheld Micro and Mini tools |
| LatticeAx™ and Small Sample Cleaver from Lattice Gear, Inc. | Tripod Polishers and ASAP-1 IPS Digital Selected Area Preparation System |
| The Cleaving Station | UltraPol End & Edge Polisher |
| EMS 150T Coater | UltraPol Basic Manual Polisher |
| Optical microscopes | Model 650 Low-Speed Diamond Saw |
| EMS Labkit - Cat #14760 | Model 920 Lapping & Polishing Machine |
| Bruker EDS | Model 865 Diamond Band Saw |
| UltraTrim Diamond Saw | Hitachi S3500 |

Faculty

1. Jerzy Gazda, PhD is a Materials Scientist with over 30 years of experience in characterization of inorganic materials. After completing his graduate work at Northwestern University, while working at Argonne National Lab, he moved to Advanced Micro Devices (AMD) in their Process Characterization & Analysis Laboratory, and then lead Electron Microscopy Department of Cerium Laboratories, LLC. In those roles, over 14 years, he taught and practiced the art of sample preparation for SEM, FIB and S/TEM from wafers, microprocessors and flash memory, and provided range to analytical services to numerous clients engaged in fabrication of MEMS and microelectronics, PV, LCD, novel materials development. He has also been conducting research into novel materials and leading new product development at TE-Connectivity, Halliburton, and at leading nanomaterials provider for Lithium Ion Batteries - Black Diamond Structures, LLC, a SABIC company, focused on development of novel nanomaterials for high energy density Lithium Ion Batteries. Jerzy also operates NanoDesigns, LLC, a consulting practice.

2. Rebecca Holdford is a consultant and annuitant of Texas Instruments, where she worked in various capacities from 1978 until 2015. Becky has worked in the semiconductor and semiconductor packaging industry for 35 years in fab process labs, device failure analysis labs, and packaging R&D groups, for both military and commercial devices. She specializes in failure analysis of packaging defects. She is a charter member of the Electronic Devices Failure Analysis Society (EDFAS), the Microscopy Society of America (MSA), Surface Mount Technology Association (SMTA) and IEEE. Becky is also a co-editor of Microelectronics Failure Analysis Desk Reference published by ASM International.
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Schedule

Tuesday, January 15, 2019

Packaged Devices
8:30-9:00 Introductory staff and participants
9:00-10:30 Definitions and Package Types
10:30-10:45 Coffee Break
10:45-12:00 Die Access Techniques: Lecture and Demo
11:00-12:00 Prepare tissues for EM processing
12:00-12:30 Provided lunch
12:30-1:30 Die Access Techniques: Hands-on
1:30-2:30 Encapsulated sections: Materials and Techniques
2:30-4:30 Un-encapsulated Sections: Equipment, Materials, and Techniques
6:00 Hosted Dinner

Wednesday, January 16, 2019

Devices on Wafer and Die Level
8:30-10:00 Seeking Targets
10:00-10:30 Workflows: Laboratory strategies and de-process overview
10:30-10:45 Coffee Break
10:45-12:00 Common Tools in Sample Prep
12:00-12:30 Provided lunch
12:30-1:30 Demonstration Laboratory
1:00-4:30 Guided Practice Laboratory I

Thursday, January 17, 2019

Practice Laboratory
8:30-12:00 Guided Practice Laboratory II
12:00-12:30 Provided lunch
12:30-4:30 Guided Practice Laboratory III

Schedule subject to change
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Registration Fee: $975.00 Includes

- Workshop syllabus
- All supplies
- Reagents and solutions
- Lunches
- Coffee
- Tea
- Dinner on the first evening of the workshop

Lodging

Participants are responsible for making their own hotel reservations.

The following hotel has been designated as the host hotel:

**Homewood Suites**
1200 Pennbrook Parkway
Lansdale, PA 19446
Phone: 215-362-6400

The special rate is $119.00 per night (plus tax) which includes a hot breakfast and a light dinner in the evening.

Please make your reservations and mention you are participating in the EMS Workshop.
GROUP CODE: EMS WORKSHOP

Everyone should plan to arrive the night before class begins.

Enrollment Note

Registration will be limited to a maximum of 15 participants.
EMS will provide samples to those who prefer not to bring their own.
Printable Registration Form

_________________________________________ M / F
Name / Title

_________________________________________
Institution

_________________________________________
Department

_________________________________________
Mailing address

_________________________________________
City / Zip

_________________________________________
Country

_________________________________________
Telephone / Fax

_________________________________________
Email:

________________________
Will you bring your own specimens? Yes / No (See Note on prior page)
What Samples are you bringing and most interested in?

________________________
All registrations must include payment.
Rate $975.00 per Person
Number of Participants ________
Total $________

Pay by check: make payable to EMS and reference “Semiconductor Workshop”.
Pay by credit card: Credit Card Type _____________________________
Credit Card Number ___________________________________________
Expiration Date ____________ 3 Digit Code ______________

________________________
Signature / Date

Return your registration to:
Stacie Kirsch
1560 Industry Road
Hatfield, PA 19440 USA
Phone: 215-412-8402
E-Mail: info@emsdiasum.com or Fax: 215-412-8452

TO REGISTER ONLINE, CLICK HERE.